IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A data-retention ~~circuitry~~ circuit comprising:

data-retention subcircuits in a feedback loop; and

a supply-switching subcircuit to decouple the data-retention subcircuits from a regular voltage supply to ~~provide~~ allow leakage current [[to]]of the data-retention subcircuits to be drawn through a well tap from a supplemental voltage supply ~~through a well tap~~ during a standby mode, the well tap comprising a conductive path coupling the data-retention subcircuits to a resistive well of a semiconductor die allowing the data-retention subcircuits to draw the leakage current from the resistive well during the standby mode.

2. (Currently Amended) The data-retention ~~circuitry~~ circuit of claim 1 further comprising an isolation subcircuit to isolate the data-retention subcircuits from a pass-gate subcircuit in response to a sleep signal,

~~wherein the supply-switching subcircuit is to switch from a regular voltage supply to the supplemental voltage supply in response to the sleep signal, and~~

wherein the isolation subcircuit is to pass data signals between the data-retention subcircuits and the pass-gate subcircuit when voltage from the regular voltage supply is present, and

wherein the isolation subcircuit and the data-retention subcircuits are outside a data path operable when voltage from the regular voltage supply is present.

3. (Currently Amended) The data-retention ~~circuitry~~ circuit of claim 1 wherein the data-retention subcircuits are to retain a state when drawing the leakage ~~receiving~~ current from the resistive well ~~supplemental voltage supply~~,

wherein the data-retention subcircuits and supply-switching subcircuits comprise semiconductor devices fabricated on the semiconductor die, and

wherein the leakage current provided through the well tap comprises primarily leakage current of the semiconductor devices comprising the data-retention subcircuits.

4. (Currently Amended) The data-retention ~~circuitry~~ circuit of claim 2 wherein the pass-gate subcircuit is to pass a latched state signal to the isolation subcircuit in response to a clock signal.

5. (Currently Amended) The data-retention ~~circuitry~~ circuit of claim 2 wherein the data-retention subcircuits, the supply-switching subcircuit and the isolation subcircuit comprise lower-leakage semiconductor devices.

6. (Currently Amended) The data-retention ~~circuitry~~ circuit of claim 2 wherein the data-retention subcircuits are coupled in series in the feedback loop, and

wherein the data-retention ~~circuitry~~ circuit further comprises an output inverter to receive a state signal from ~~one of~~ either the isolation subcircuit or the pass-gate subcircuit and to provide an output signal.

7. (Currently Amended) The data-retention ~~circuitry~~ circuit of claim 1 wherein the supply-switching subcircuit comprises a semiconductor switching subcircuit that is part of [[a]]the semiconductor die~~, the semiconductor die having a well-tap to provide the current from the supplemental voltage supply~~, ~~and~~

wherein the semiconductor switching subcircuit is to couple the data-retention subcircuits to the regular voltage supply when the semiconductor switching subcircuit receives a first state of [[the]]a sleep signal, and

wherein the leakage current is drawn by ~~to flow to~~ the data-retention subcircuits from the well tap ~~well-tap~~ when the semiconductor switching subcircuit receives a second state of the sleep signal.

8. (Cancelled)

9. (Currently Amended) The data-retention ~~circuitry~~ circuit of claim 2 further comprising a master latch to latch a state signal, [[and]]

wherein the pass-gate subcircuit, the data-retention subcircuits, the isolation subcircuit and the supply-switching subcircuit are part of a slave latch, and

wherein the pass-gate subcircuit is to pass the latched state signal to the isolation subcircuit from the master latch in response to a clock signal.

10. (Currently Amended) The data-retention ~~circuitry~~ circuit of claim 9 wherein circuits of the master latch are to receive power from the regular voltage supply, and

wherein during the standby mode the regular voltage supply is turned off.

11. (Currently Amended) The data-retention ~~circuitry~~ circuit of claim [[9]] 1 further comprising an isolation subcircuit to isolate the data-retention subcircuits from a pass-gate subcircuit in response to a sleep signal,

wherein the data-retention subcircuits, the supply-switching subcircuit and the isolation subcircuit comprise lower-leakage semiconductor devices, and

wherein the pass-gate subcircuit ~~and master latch~~ comprises higher-leakage semiconductor devices, the lower-leakage devices having at least one of ~~either~~ a longer channel length, a thicker gate-oxide layer or a higher threshold voltage than the higher-leakage semiconductor devices.

12. (Currently Amended) A processing system comprising:

a processor on a semiconductor die; and

a data-retention ~~circuitry~~ circuit on the semiconductor die to retain state information for the processor during a standby mode, wherein the data-retention ~~circuitry~~ circuit ~~comprise~~ comprises data-retention subcircuits to draw leakage ~~receive~~ current through a well tap in the semiconductor die during the standby mode to retain the state information,

wherein the well tap comprises a conductive path coupling the data-retention subcircuits to a resistive well of the semiconductor die.

13. (Currently Amended) The system of claim 12 wherein the data-retention ~~circuitry~~ circuit further comprises an isolation subcircuit to isolate the data-retention subcircuits from a pass-gate subcircuit in response to a sleep signal, and a supply-switching subcircuit to decouple the data-retention subcircuits from a regular voltage supply to ~~provide~~ allow leakage current of [[to]] the data-retention subcircuits to be drawn from a supplemental voltage supply through the well tap from the resistive well during the standby mode,

wherein the isolation subcircuit and the data-retention subcircuits are outside a data path operable when voltage from the regular voltage supply is present.

14. (Currently Amended) The system of claim 12 wherein the data-retention ~~circuitry~~ subcircuits are arranged in cells on the semiconductor die, the cells having at least one well tap to provide the leakage current from the supplemental voltage supply,

wherein the data-retention subcircuits and supply-switching subcircuits comprise semiconductor devices fabricated on the semiconductor die, and

wherein the leakage current provided through the well tap comprises primarily leakage current of the semiconductor devices comprising the data-retention subcircuits.

15. (Currently Amended) The system of claim 13 ~~wherein the supply-switching subcircuit is to switch from a regular voltage supply to the supplemental voltage supply in response to a sleep signal, and~~ wherein the isolation subcircuit is to pass data signals between the data-retention subcircuits and the pass-gate subcircuit when voltage from the regular voltage supply is provided.

16. (Original) The system of claim 13 wherein the pass-gate subcircuit is to pass a latched state signal to the isolation subcircuit in response to a clock signal.

17. (Currently Amended) The system of claim 16 wherein the data-retention ~~circuitry~~ circuit further comprises a master latch to latch a state signal, [[and]]

wherein the pass-gate subcircuit, the data-retention subcircuits, the isolation subcircuit and the supply-switching subcircuit are part of a slave latch, and

wherein the pass-gate subcircuit is to pass the latched state signal to the isolation subcircuit from the master latch in response to a clock signal.

18. (Original) The system of claim 17 wherein circuits of the master latch are to receive current from the regular voltage supply, and

wherein during the standby mode the regular voltage supply is turned off.

19. (Currently Amended) The system of claim [[17]] 12 further comprising an isolation subcircuit to isolate the data-retention subcircuits from a pass-gate subcircuit in response to a sleep signal,

wherein the data-retention subcircuits, the supply-switching subcircuit and the isolation subcircuit comprise lower-leakage semiconductor devices, and wherein the pass-gate subcircuit ~~and the master latch~~ comprises higher-leakage semiconductor devices, the lower-leakage devices having at least one of ~~either~~ a longer channel length, a thicker gate-oxide layer or a higher threshold voltage than the higher-leakage semiconductor devices.

20. (Currently Amended) A method comprising:

isolating data-retention subcircuits in response to a sleep signal;

~~switching~~ decoupling the data-retention subcircuits from a regular ~~to receive current from a supplemental~~ voltage supply in response to the sleep signal to allow the data-retention subcircuits to draw leakage current through a well tap from a supplemental voltage, the well tap comprising a conductive path coupling the data-retention subcircuits to a resistive well of a semiconductor die; [[and]]

retaining state information by the data-retention subcircuits when drawing ~~receiving~~ the leakage current from the supplemental voltage supply during a standby mode.

21. (Currently Amended) The method of claim 20 ~~further comprising providing the current from the supplemental voltage supply through a well-tap on a semiconductor die.~~ wherein the isolating is performed by an isolation subcircuit, and

wherein the isolation subcircuit and the data-retention subcircuits are outside a data path operable when voltage from the regular voltage supply is present.

22. (Currently Amended) The method of claim 20 wherein switching further comprises switching on ~~from a regular voltage supply to~~ the supplemental voltage supply in response to the sleep signal,

wherein the data-retention subcircuits and supply-switching subcircuits comprise semiconductor devices fabricated on the semiconductor die, and

wherein the leakage current provided through the well tap comprises primarily leakage current of the semiconductor devices comprising the data-retention subcircuits.

23. (Original) The method of claim 22 further comprising passing state information between the data-retention subcircuits and a pass-gate subcircuit when the regular voltage supply is present at an isolation subcircuit.

24. (Withdrawn – Currently Amended) A wireless communication device comprising:

an omnidirectional antenna to communicate radio-frequency signals;

a processor on a semiconductor die to convert between the radio-frequency signals and data signals; and

a data-retention ~~circuitry~~ circuit on the semiconductor die to retain state information for the processor during a standby mode, wherein the data-retention ~~circuitry~~ circuit ~~comprise~~ comprises data-retention subcircuits to receive current through a well tap in the semiconductor die during the standby mode to retain the state information.

25. (Withdrawn – Currently Amended) The device of claim 24 wherein the data-retention ~~circuitry~~ circuit further comprises an isolation subcircuit to isolate the data-retention subcircuits from a pass-gate subcircuit in response to a sleep signal, and a supply-switching subcircuit to provide current to the data-retention subcircuits from a supplemental voltage supply through a well tap during the standby mode.

26. (Withdrawn – Currently Amended) The device of claim 25 wherein the data-retention subcircuits, the switching subcircuit and the isolation subcircuit comprise lower-leakage semiconductor devices, and wherein the pass-gate subcircuit comprises higher-leakage semiconductor devices, the lower-leakage devices having at least one of a longer channel length, a thicker gate-oxide layer or a higher threshold voltage than the higher-leakage semiconductor devices.

27. (New) A data-retention circuit comprising:

data-retention subcircuits in a feedback loop;

a supply-switching subcircuit to decouple the data-retention circuits from a regular voltage supply and to allow the data-retention subcircuits to draw leakage current from a supplemental voltage supply through a well tap during a standby mode, the well tap comprising a conductive path to a resistive well of a semiconductor die;

an isolation subcircuit to isolate the data-retention subcircuits from a pass-gate subcircuit in response to a sleep signal; and

a master latch to latch a state signal,

wherein the supply-switching subcircuit is to switch from the regular voltage supply in response to the sleep signal,

wherein the isolation subcircuit is to pass data signals between the data-retention subcircuits and the pass-gate subcircuit when voltage from the regular voltage supply is present,

wherein the pass-gate subcircuit, the data-retention subcircuits, the isolation subcircuit and the supply-switching subcircuit are part of a slave latch,

wherein the pass-gate subcircuit is to pass the latched state signal to the isolation subcircuit from the master latch in response to a clock signal,

wherein the data-retention subcircuits, the supply-switching subcircuit and the isolation subcircuit comprise lower-leakage semiconductor devices, and

wherein the pass-gate subcircuit and master latch comprise higher-leakage semiconductor devices, the lower-leakage devices having at least one of a longer channel length, a thicker gate-oxide layer or a higher threshold voltage than the higher-leakage semiconductor devices.

28. (New) A processing system comprising:

a processor on a semiconductor die; and

a data-retention circuit on the semiconductor die to retain state information for the processor during a standby mode, the data-retention circuit comprising data-retention subcircuits to draw leakage current through a well tap in the semiconductor die during the standby mode to retain the state information the well tap comprising a conductive path to a well of the semiconductor die,

wherein the data-retention circuit further comprises an isolation subcircuit to isolate the data-retention subcircuits from a pass-gate subcircuit in response to a sleep signal, and a supply-switching subcircuit to decouple the data-retention subcircuits from a regular voltage supply in response to the sleep signal to allow the data-retention subcircuits to draw the leakage current from a supplemental voltage supply through the well tap during the standby mode,

wherein the pass-gate subcircuit is to pass a latched state signal to the isolation subcircuit in response to a clock signal,

wherein the data-retention circuit further comprises a master latch to latch a state signal,

wherein the pass-gate subcircuit, the data-retention subcircuits, the isolation subcircuit and the supply-switching subcircuit are part of a slave latch,

wherein the pass-gate subcircuit is to pass the latched state signal to the isolation subcircuit from the master latch in response to the clock signal,

wherein the data-retention subcircuits, the supply-switching subcircuit and the isolation subcircuit comprise lower-leakage semiconductor devices, and

wherein the pass-gate subcircuit and the master latch comprise higher-leakage semiconductor devices, the lower-leakage devices having at least one of either a longer channel length, a thicker gate-oxide layer or a higher threshold voltage than the higher-leakage semiconductor devices.